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Code No: A7004

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, March/April-2011
VLSI ARCHITECTURE AND DESIGN METHODOLOGIES
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. a. Explain the Finite-State machine approach for VLSI Design methodology.
   b. Explain the simulation and verification methods at the system level. [12]

2. a. Explain the pipelining architecture implementation in advanced processors
   b. Explain different memory systems in VLSI Design. [12]

3. a. Explain the data flow for a multiprocessor arrays.
   b. Explain the systolic arrays method. [12]

4. a. Explain the method of clock generation
   b. Explain the methods of buffering and clock distribution. [12]

5. a. Explain different programming techniques in FPGA
   b. What is mean by device dependant and device independent technology in FPGA design? [12]

6. a. Explain the standard CPLD structure
   b. What are the different CPLD's available in the Industry. Give examples. [12]

7. Explain the design methodology for low power design. [12]

8. Write Short notes on any **two** of the following.
   a. VLSI design approach in super computing.
   b. VLSI design approach in image processing.
   c. PLA design. [12]

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